Artificial Intelligence Exploration (AIE) Opportunity
DARPA-PA-19-03-03
Hyper-Dimensional Data Enabled Neural Networks (HyDDENN)

I. Opportunity Description

The Defense Advanced Research Projects Agency (DARPA) is issuing an Artificial Intelligence Exploration (AIE) Opportunity, inviting submissions of innovative basic or applied research concepts in the technical domain of automated knowledge discovery, curation, and application. This AIE Opportunity is for the Hyper-Dimensional Data Enabled Neural Networks (HyDDENN) program and is being issued under the Program Announcement for AIE, DARPA-PA-19-03. All proposals in response to this AIE Opportunity will be submitted to DARPA-PA-19-03-03. All awards will be made in the form of an Other Transaction (OT) for prototype project. The total award value for the combined Phase 1 base and Phase 2 option is limited to $1,000,000. This total award value includes Government funding and performer cost share, if required or if proposed.

A. Introduction

In a quest for higher accuracies, state-of-the-art (SOA) Deep Neural Networks (DNN) are growing wider and deeper, with the complexity growing from millions to hundreds of millions of parameters in the last few years.[1] The basic computational primitive to execute training and inference functions in DNN is the multiply and accumulate (MAC) operation. As DNN parameter count increases, SOA networks require tens of billions of MAC operations to carry out one inference.[2] As a result, the accuracy of DNN is fundamentally limited by available MAC resources.[1] Consequently, SOA high accuracy DNNs are hosted in the cloud centers with clusters of energy hungry processors to speed up processing. This compute paradigm will not satisfy many DoD applications which demand extremely low latency, high accuracy artificial intelligence (AI) under severe size, weight, and power constraints.

B. Objective/Scope

The HyDDENN program seeks new data enabled neural network (NN) architectures to break the reliance on large MAC-based DNNs. HyDDENN will explore and develop innovative data representations with shallow NN architectures based on efficient, non-MAC, digital compute primitives to enable highly accurate and energy efficient AI for DoD edge systems.

HyDDENN seeks to explore the impact of dimensionality and network complexity on output accuracy during both the network design, training and inference.

1. HyDDENN will explore the impact of dimensionality and network complexity (parameter count) on the ultimate trained accuracy of a shallow hyper-dimensional (HD) NN.
2. HyDDENN will demonstrate robust HD NN processing over noisy input when performing inference for a given application edge application.

The goal of HyDDENN is to significantly reduce AI hardware complexity by reducing parameter count by at least 10x, while maintaining SOA accuracy in comparison with a similar MAC-based DNN solution. It is expected that the resulting compute NN element will directly operate on the

[1] "EfficientNet: Rethinking Model Scaling for Convolutional Neural Networks" *Mingxing Tan, Quoc Le; Proceedings of the 36th International Conference on Machine Learning, PMLR 97:6105-6114, 2019.*

[2] "AutoML for large scale image classification and object detection" ai.googleblog.com; goo.gl/F6QXBd (2017)

new HD data representation using simple integer or binary compute primitives (such as bitwise XOR, XNOR, etc.) rather than the MAC. With efficient digital compute hardware, these innovations will lead to at least 100x reduction in combined compute power and throughput, while retaining high-accuracy output when compared to the SOA DNN approach.

Several recent innovations have motivated this exploration:

- Hyper-dimensional data representations have been shown to outperform standard machine learning implementations in terms of accuracy in some modestly scaled applications.[3]
- Hyper dimensional data representation was demonstrated recently to efficiently encode and decode highly complex ($2^{1,000}$) orthogonal binary vectors with linear scalability, more efficiently than other mainstream approaches.[4]
- New training methods have been implemented and simulated in shallow but wide networks such as restricted Boltzmann or approximate full Boltzmann machines with high accuracy, which could lead to lower parameter counts.[5]
- New data representations with efficient primitive logic operations were implemented on binary bitwise XOR hardware. Reducing reliance on MAC operations in non-von Neumann architectures demonstrated orders of magnitude less energy consumption per inference in simulation.[6]

By representing input data in sparse HD vectors, emerging HD compute theory predicts NNs processing these data structures will exhibit high accuracy inference and robustness to transmission and computing errors. HD data representation may enable efficient in-memory compute based on simple hardware realization in high-throughput digital compute primitives. HyDDENN will explore and benchmark the advantages of HD compute in accuracy, latency, network size, and physical implementation against SOA DNNs performing similar tasks and workload in relevant DoD edge AI applications, such as communications and sensing.

C. Structure

Proposals submitted in response to this AIE opportunity, DARPA-PA-19-03-03, must be UNCLASSIFIED, and must address two independent and sequential effort phases: a Phase 1 Feasibility Study (base) and a Phase 2 Proof of Concept (option). The periods of performance for these phases are 6 months for the Phase 1 base effort and 12 months for the Phase 2 option effort. Combined Phase 1 base and Phase 2 option efforts for this AIE Opportunity should not exceed 18 months. The Phase 1 (base) award value should not exceed $300,000. The Phase 2 (option) award value should not exceed $700,000. The total award value for the combined Phase 1 and Phase 2 is limited to $1,000,000. This total award value includes Government funding and performer cost share, if required or if proposed.

Phase 1 studies will be evaluated to determine the feasibility of the approach and whether to continue the option for Phase 2.

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[3] "Adventures in HD Computing" Lund Circuits Workshop: Presentation Jan Rabaey; September 25 2018.
[4] "BRIC: Locality-based Encoding for Energy-Efficient Brain-Inspired Hyperdimensional Computing" Imani, Rosing et al. DAC' 19, June2-6, 2019.
[5] Combining Learned Representations for Combinatorial Optimization; *Saavan Patel, Sayeef Salahuddin* (https://arxiv.org/abs/1909.03978).
[6] "Brain-Inspired Computing Exploiting Carbon Nanotube FETs and Resistive RAM: Hyperdimensional Computing Case Study" ISSCC 2018; Mitra et. al.

D. HyDDENN Technical Description

The HyDDENN program will establish new data representations and compute primitives to represent AI in shallow neural networks for efficient hardware at the edge. This will provide SOA accuracy at a latency that cannot be achieved through secured remote access to cloud computing located far from the edge. This will be achieved through the following technical approach.

HyDDENN AI Exploration Steps:

1. Explore the impact of dimensionality, sparsity and numerical precision on accuracy and performance by comparing the same task while varying the encoding dimensionality ($500 < D < \sim 10{,}000$) of HD vectors.
2. Use the optimized HD NN to demonstrate the improvement of efficiency of HD encoding and associated resource requirements for training and interference when mapped to an efficient, non-MAC based, compute primitive.
3. Demonstrate the required hardware complexity to store and process the proposed dimensionality of HD hypervectors in field programmable gate arrays (FPGAs) and future ASIC embedded devices.

HyDDENN Program Overview

Phase 1 - Methodology: Proposers will demonstrate their proposed edge applications with innovative approaches in the following methodology:

1. Develop efficient vector encoding and decoding scheme.
2. Train a HyDDENN network (using one or few pass training if possible).
3. Perform inference using associative search classification or datastream decoding to compare class vectors and input vectors based on a vector distance measurement such as cosine distance, Hamming distance, or some other equivalent difference measurement to measure accuracy. Provide analysis on the trade-off in dimensionality of HD data representation and network size in order to provide a prescribed output accuracy. Analyze the impact of HD dimensionality and network size on the inference accuracy of noisy input data of the proposed HD NN.
4. Demonstrate contextual data interpretation through vector decoding and identification of key vectors based on degree of similarity or difference. Provide analysis on the capability of prediction of future events from identified data fragments or from highly noisy data.

Key Demonstration: Demonstration of HD NN accuracy with reduced parameter counts and low complexity compute primitive.

Phase 2 - Implementation: Proposers should detail their approach to implementing the proposed application in a hardware demonstration:

1. Implement a prototype test bench demonstration of targeted HD neural network application in real-time with low-latency, utilizing FPGAs and/or other commercial off the shelf (COTS) electronic components.
2. Develop an ASIC architecture and high level logic designs at RTL level as well as a project plan to implement a future fully programmable integrated chip-scale digital IC with the proposed HD data representation, logic primitives, and shallow HD NN to attain the HyDDENN performance goals and metrics for the targeted application.

Key Demonstration: Demonstration and performance projections in benchtop demo and projection to custom digital IC from design simulation.

HyDDENN Applications

Novel high dimensional data representations combined with efficient computing architectures will enable streaming sparse data flows, with the capability for efficient contextual classification from fragmental segments of data with high accuracy at the edge. Each HyDDENN proposal should propose an application to best illustrate the measurable advantages in reduction of network parameters, scalability, processing latency, simplification of compute primitives, and operations as well as the power reduction for the proposed digital hardware implementation. If necessary, proposers should emphasize a plan to establish a dataset that does not contain personally identifiable information (PII) to validate the proposed solution. It is expected that HyDDENN will have significant impact in the areas of edge/IoT communications and contextual edge sensing and classification. Some topic of interests are illustrated below; however, proposers may propose other DoD-relevant applications that would demonstrate similar capabilities and benefits. Examples of applications of interests include, but are not limited to:

1) Contextual communications for edge/IOT
    a) Efficient cognitive communications
    b) Efficient sensing and processing of RF signals

2) Efficient contextual edge sensing and classification
    a) Speech recognition and context generation
    b) Object relationships from images for context generation
    c) Language recognition and context generation
    d) Activity recognition and context generation
    e) Gesture recognition and context generation
    f) Facial recognition and context generation
    g) Medical diagnostics and context generation

E. Schedule/Milestones

Proposers must address the following Research Project Objectives, metrics, and deliverables, along with fixed payable milestones in their proposals. The task structure must be consistent across the proposed schedule, Task Description Document (TDD), and the Volume 2 - Price Volume. Proposers must complete the "Schedule of Milestones and Payments" excel Attachment provided with this AIE Opportunity as part of submitting a complete proposal and fulfilling the requirements under Vol. 2 Price Volume. If selected for award negotiation, the fixed payable milestones will be directly incorporated into Attachment 2 of the OT for Prototype agreement ("Schedule of Milestones and Payments"). Proposers are encouraged to use the TDD template provided with the Program Announcement DARPA-PA-19-03, which will be Attachment 1 of the OT agreement.

For planning and budgetary purposes, proposers should assume a program start date of February 12, 2020. Schedules will be synchronized across performers, as required, and monitored/revised as necessary throughout the effort. Proposals must include delivery schedules for Phase 1 and Phase 2 that include timelines for preliminary (to facilitate inspection by the Program Manager) and final (to facilitate evaluation) release of deliverables. Research objectives and fixed milestones for this program should include:

Phase 1 Research Objectives:
Establish HyDDENN: Develop the machine learning architecture, data representation, algorithm, compute primitives, neural network topology, dataset and simulation to show the initial accuracy and power projections for the proposed application.

- Establish new HD data representations, digital compute primitives, and accurate shallow NN architectures for a specified application. Include analysis of network precision vs. required dimensionality.
- Curate edge application dataset.
- Compare application accuracy in simulation vs. SOA DNN approaches.
- Estimate power consumption and other metrics expected in Phase 2 COTS hardware implementation for proposed edge sensing or communications application.

The outcome of Phase 1 efforts will result in a preliminary design of the prototype system including the delivery of the architecture, HD data representation, algorithms, compute primitives, primitives, neural network topology, hardware configuration, and performance analysis of the proposed edge applications.

Phase 1 Milestones:

- Milestone #1 (Month 1): Provide a comprehensive description of the proposed application, hyper-dimensional data representations, associated shallow neural network architecture and simplified compute primitive, with in-depth support of published literature. Include an overview and comparison of current state of the art pertaining to the proposed approach and an initial description of the dataset that will be used for comparison. Describe the planned architecture on how the HD data representation, algorithm and hardware approach will meet required performance and functionalities of the targeted application. Specify what further information/analysis will be performed by Milestone #2 to develop a working simulation of the architecture and all other relevant details.
- Milestone #2 (Month 3): Provide an interim report describing the initial simulation of the neural network architecture and initial accuracy numbers in comparison with SOA DNN implementing the same dataset. Specify what further information/analysis will be performed by Milestone #3 to develop a final working simulation of the architecture and all other relevant details.
- Milestone #3 (Month 5): Demonstrate simulated performance of the proposed HD NN to enabled by a shallow neural network with 10x parameter reduction and accuracy comparable to SOA DNN approach of the proposed application and data set. Submit Phase 1 Final Report in preparation for Phase 2 option. Phase 1 final report should include the trade studies of the accuracy of the proposed HD NN in terms of the required HD data dimensionality and network size to process noisy data. It should summarize an approach for FPGA-based hardware implementation and test bench demonstration, as well as initial mapping to digital hardware and a high level digital hardware design for future ASIC edge implementation. The report should include a description of the targeted application and procured dataset to provide a comparison with the established state of the art including quantifiable performance metrics, such as accuracy, dimensionality, and robustness for the proposed application.

Phase 2 Research Objectives:
Hardware Design Study: Implement a high level programmable hardware design to estimate the potential benefits of custom ASIC hardware for the proposed application, including an exploration of edge applications in communications and sensing.

- Prototype Emulation in COTS Hardware: Implement and demonstrate a prototype test bench with the Phase 1 designs in an FPGA and/or with COTS components, to emulate the HyDDENN NN and verify associated performance metrics for the proposed application.
- Project Plan: Develop a design and project plan to implement a future full programmable integrated chip-scale ASIC with SOA machine learning solution to attain the HyDDENN performance goals and metrics for the targeted application as well as generally reprogrammable to other HD NN tasks.

The outcome of Phase 2 will result in a demonstration of the prototype system to attain the targeted performance metrics as well as the future project plan including optimized architecture, HD data representation, NN topology, algorithms, compute primitive, supporting simulation, performance analysis and documentation for a future fully programmable integrated ASIC hardware design.

Phase 2 Milestones:
- Milestone #4 (Month 7): Report on lessons learned, updated architectures algorithms, hardware implementation of prototype testbench, and performance evaluation metrics of targeted application for Phase 2 development.
- Milestone #5 (Month 9): Report describing initial FPGA simulation results, preparation of COTS hardware prototype components, and integration plan of hardware with software and mapping to efficient digital hardware primitives.
- Milestone #6 (Month 11): Interim FPGA code release and demonstration of emulated system showing performance for real-world system/processes. Report on initial testing of hardware components and the integration of software with hardware for the application demonstration. Report detailing high level hardware design.
- Milestone #7 (Month 13): Interim report quantifying system performance, comparing to alternative state-of-the art approaches based on both FPGA simulation and estimated ASIC implementation. Report on preliminary testing of assembled prototype test bench for targeted application.
- Milestone #8 (Month 15): Live demonstration of prototype test bench system to illustrate the performance for real-world system/process of the proposed application using a COTS FPGA in conjunction with other processors.
- Milestone #9 (Month 18): Final release of FPGA code and data set. Provide Phase 2 report to document the HyDDENN architecture, HD data representations, algorithms, neural network topology, hardware implementation, FPGA code, data set, and measured performance metrics of demonstrated prototype test bench for the proposed application and data set. Document the comparison of the demonstrated performance metrics with initial simulation, data set, and alternative methods including the quantification of hardware reduction factors, accuracy, latency, robustness, stability, and scalability of functionalities and size/weight/power for real world practice at the edge. Provide comprehensive documentation for the future ASIC design

of architectures, algorithms, methods, simulated results, as well as associated cost and schedule to implement them for future chip-scale integrated system.

All proposals must include the following meetings and travel in the proposed schedule and cost:

- To foster collaboration between teams and disseminate HyDDENN AIE opportunity developments, a two-day Principal Investigator (PI) meeting will be held approximately every six months after the kickoff meeting. For budgeting purposes, plan for four two-day meetings over the course of 18 months: two meetings in the Washington, D.C. area (Month 1 and Month 12) and two meetings in the San Francisco, CA area (Month 6 and Month 18).
- Regular teleconference meetings will be scheduled with the Government team for progress update, as well as for problem identification and mitigation. These are expected to occur within 2 weeks of each milestone due date and will be attended by the government Agreement Officer's Representative (AOR) as a requirement to approve milestone payment.
- Proposers should anticipate at least one site visit per phase by the DARPA Program Manager. At that time, performers will have the opportunity to update and demonstrate progress towards agreed-upon milestones.
- Proposers should plan travel for GOMACTech 2021 and participation in a joint HyDDENN session detailing their non-proprietary results for interested government transition partners.
- Proposers may plan travel for one technical conference per year.

F. Metrics/Deliverables

Quantitative Metrics:

Maintain SOA accuracy (relative to a SOA MAC-based DNN implementation) while achieving better than:

- 10x reduction in network complexity (number of parameters)
- 10x simpler digital logic operations than MAC (as measured by compute cycles)
- 100x reduction in combined latency and projected power from application-specific integrated circuit (ASIC) implementation, computing the selected HyDDENN communication and edge sensing applications. These gains are expected based on simplified compute primitive, processing operations, and reduced memory access, when compared to SOA MAC-based DNN implementation.
- HD vectors with dimension ≥ 500

Performers will be expected to provide at a minimum the following deliverables:

Phase 1:

- Fully simulated shallow neural network using hyper-dimensional data representation trained to achieve SOA inference accuracy when compared with a SOA DNN.
- Final Phase 1 Report summarizing targeted application, technical approach, prototype architectures, HD data representation, algorithms, shallow NN topology, data sets, and simulated results. Documentation of the performance comparison to alternative SOA methodology, quantification of accuracy, quantification of robustness. Summary of preliminary FPGA emulation of critical compute blocks.
- All other reports and data as required by the individual Phase 1 milestones.

Phase 2:

- Live demonstration of proposed communication or edge sensing application showing real-time processing on prototype test bench using COTS FPGA and other electronic components.
- Final FPGA code and dataset of COTs components (if applicable).
- Preliminary ASIC hardware architecture design with estimated latency and power consumption for future chip-scale implementation at the edge. Trade space analysis of compute resources required to implement shallow HD networks of varying dimensionality and number of parameters to provide a general purpose solution for a wide variety of applications with a target error rate less than 10^{-3} in the output.
- Final Phase 2 report documenting technical approach, architectures, HD data representation, compute primitives, algorithms, shallow NN topology, data set, COTS emulation, and measured performance. Report should provide comparisons with alternative approaches with quantification on the accuracy, latency, scalability, and estimated power for the proposed application.
- All other deliverables as required by the individual Phase 2 milestones such as registered reports on milestones, experimental protocols, publications, IP inventions, intermediate and final versions of hardware and hardware designs, software libraries, code, and APIs, including documentation and user manuals, and/or a comprehensive assemblage of design documents, models, modeling data and results, and model validation data.

Unless otherwise specified, all deliverables are expected to be released with unlimited rights.

II. Award Information

Selected proposals that are successfully negotiated will result in award of an OT for Prototype agreement. See Section 3 of the AIE Program Announcement (DARPA-PA-19-03) for information on awards that may result from proposals submitted in response to this notice.

Proposers must review the model OT for Prototype agreement provided as an attachment to the AIE Program Announcement (DARPA-PA-19-03) prior to submitting a proposal. DARPA has provided the model OT in order to expedite the negotiation and award process, and ensure DARPA achieves the goal of AIE, which is to enable DARPA to initiate a new investment in less than 90 days from idea inception. The model OT is representative of the terms and conditions that DARPA intends to award for all AIE awards. The task description document, schedule of milestones and payments, and data rights assertions requested under Volume 1, Volume 2, and Volume 3 of the AIE solicitation will be included as attachments to the OT agreement upon negotiation and award.

Proposers may suggest edits to the model OT for consideration by DARPA and provide a copy of the model OT with track changes as part of their proposal package. Please note that suggested edits may not be accepted by DARPA. The Government reserves the right to remove a proposal from award consideration should the parties fail to reach agreement on OT award terms and conditions. If edits to the model OT are not provided as part of the proposal package, DARPA assumes that the proposer has reviewed and accepted the award terms and conditions to which they may have to adhere, indicating agreement (in principle) with the listed terms and conditions applicable to the specific award instrument.

In order to ensure that DARPA achieves the AIE goal of award within 90 days from the posting date (November 12, 2019) of this announcement, DARPA reserves the right to cease negotiations when an award is not executed by both parties (DARPA and the selected organization) on or before February 7, 2020.

III. Eligibility

See Section 4 of the AIE Program Announcement (DARPA-PA-19-03) for information on who may be eligible to respond to this notice.

IV. AIE Opportunity Responses

Responses to this HyDDENN opportunity must be submitted as full proposals to DARPA-PA-19-03-03 as described therein. All proposals must be UNCLASSIFIED.

A. Proposal Content and Format

All proposals submitted in response to this notice must comply with the content and format instructions in Section 5 of the AIE Program Announcement (DARPA-PA-19-03). All proposals must use the templates that have been provided as attachments to the PA and follow the instructions therein.

Information submitted but not explicitly requested in the AIE Program Announcement (DARPA-PA-19-03), its attachments, or this notice (HyDDENN DARPA-PA-19-03-03) may not be evaluated.

B. Proposal Submission Instructions

Responses to DARPA-PA-19-03-03shall be submitted through electronic upload to DARPA's BAA Portal (https://baa.darpa.mil).

DARPA will acknowledge receipt of complete submissions via email and assign identifying numbers that should be used in all further correspondence regarding those submissions. If no confirmation is received within two business days, please contact HyDDENN@darpa.mil to verify receipt.

When planning a response to this AIE Opportunity, proposers should take into account the submission time zone and that some parts of the submission process may take from one business day to one month to complete (e.g., registering for a Data Universal Numbering System (DUNS) number or Tax Identification Number (TIN).

Electronic Upload

First time users of the DARPA BAA Portal must complete a two-step account creation process. The first step consists of registering for an extranet account by going to the URL listed above and selecting the "Account Request" link. Upon completion of the online form, proposers will receive two separate emails; one will contain a user name and the second will provide a temporary password. Once both emails have been received, the second step requires proposers to go back to the submission website and log in using that user name and password. After accessing the extranet, proposers may then create a user account for the DARPA Submission website by selecting the

"Register your Organization" link at the top of the page. Once the user account is created, proposers will be able to see a list of solicitations open for submissions, view submission instructions, and upload/finalize their proposal.

Proposers who already have an account on the DARPA BAA Portal may simply log in at https://baa.darpa.mil, select this solicitation from the list of open DARPA solicitations and proceed with their proposal submission. Note: proposers who have created a DARPA Submission website account to submit to another DARPA Technical Office's solicitations do not need to create a new account to submit to this solicitation.

All full proposals submitted electronically through the DARPA Submission website must meet the following requirements: (1) uploaded as a zip file (.zip or .zipx extension); (2) only contain the document(s) requested herein; (3) only contain unclassified information; and (4) must not exceed 100 MB in size. Only one zip file will be accepted per full proposal. Full proposals not uploaded as zip files will be rejected by DARPA. Technical support for the DARPA Submission website is available during regular business hours, Monday – Friday, 9:00 a.m. – 5:00 p.m. Requests for technical support must be emailed to BAAT_Support@darpa.mil with a copy to HyDDENN@darpa.mil. Questions regarding submission contents, format, deadlines, etc. should be emailed to HyDDENN@darpa.mil. Questions/requests for support sent to any other email address may result in delayed/no response.

Since proposers may encounter heavy traffic on the web server, DARPA discourages waiting until the day proposals are due to request an account and/or upload the submission. Note: Proposers submitting a proposal via the DARPA Submission site MUST (1) click the "Finalize" button in order for the submission to upload AND (2) do so with sufficient time for the upload to complete prior to the deadline. Failure to do so will result in a late submission.

C. Proposal Due Date and Time

Proposals in response to this notice are due no later than **December 11, 2019 at 12:00 noon (ET)**. Full proposal packages as described in Section 5 of the AIE Program Announcement (DARPA-PA-19-03) must be submitted per the instructions outlined therein *and received by DARPA* no later than the above date and time. Proposals received after this date and time will not be reviewed.

Proposers are warned that submission deadlines as outlined herein are strictly enforced. Note: some proposal requirements may take from 1 business day to 1 month to complete.

V. Proposal Evaluation and Selection

Proposals will be evaluated and selected in accordance with Section 6 of the AIE Program Announcement (DARPA-PA-19-03). Proposers will be notified of the results of this process as described in Section 7.1 of DARPA-PA-19-03.

VI. Administrative and National Policy Requirements

Section 7.2 of DARPA-PA-19-03 provides information on Administrative and National Policy Requirements that may be applicable for proposal submission as well as performance under an award.

VII. Point of Contact Information

Dr. Young-Kai Chen, Program Manager, DARPA/MTO, HyDDENN@darpa.mil

VIII. Frequently Asked Questions (FAQs)

All technical, contractual, and administrative questions regarding the HyDDENN AIE opportunity must be emailed to HyDDENN@darpa.mil. Emails sent directly to the Program Manager or any other address may result in delayed or no response.

All questions must be in English and must include name, email address, and the telephone number of a point of contact. DARPA will attempt to answer questions publically in a timely manner; however, questions submitted within 7 days of the proposal due date and time listed herein may not be answered.

If needed, DARPA will post a HyDDENN FAQ list under the AIE Opportunity on the DARPA/MTO Opportunities page at https://www.darpa.mil/work-with-us/opportunities?tFilter=&oFilter=3&sort=name. The list will be updated on an ongoing basis until one week prior to the proposal due date and time. In addition to the FAQ specific to this notice, proposers should also review the AIE General FAQ list on the DARPA/DSO Opportunities page under the Program Announcement for AIE (DARPA-PA-19-03).